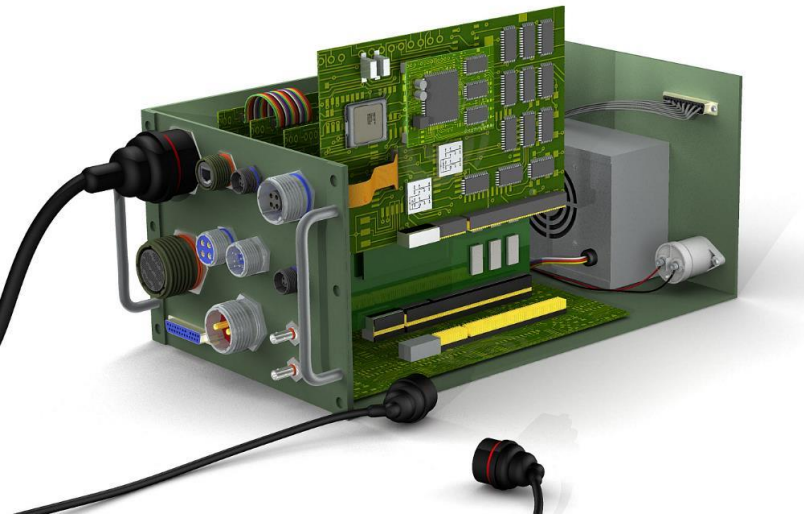




# Evolving Interconnect Standards – Keeping Pace with the Embedded Computing Industry

*Inventing. Connecting. Inspiring. Thriving.*

Michael Walmsley  
Standards and Product Management  
Aerospace Defense and Marine Business Unit



EVERY CONNECTION COUNTS



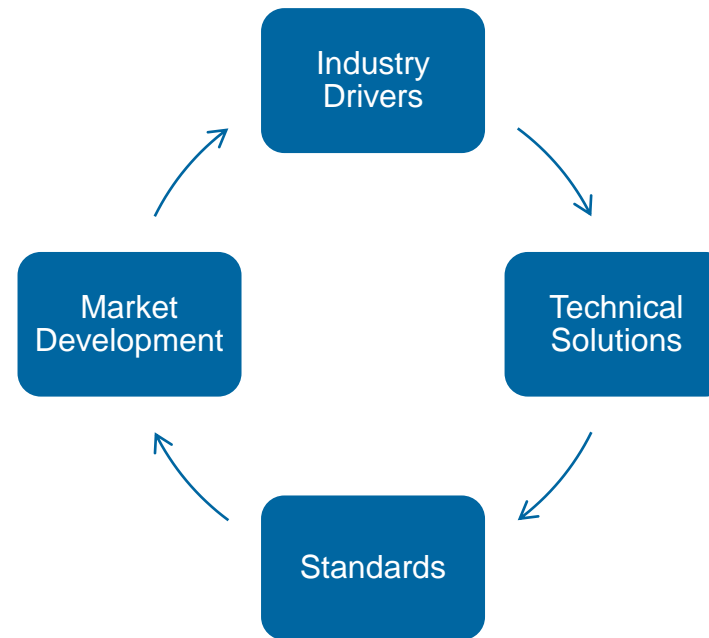
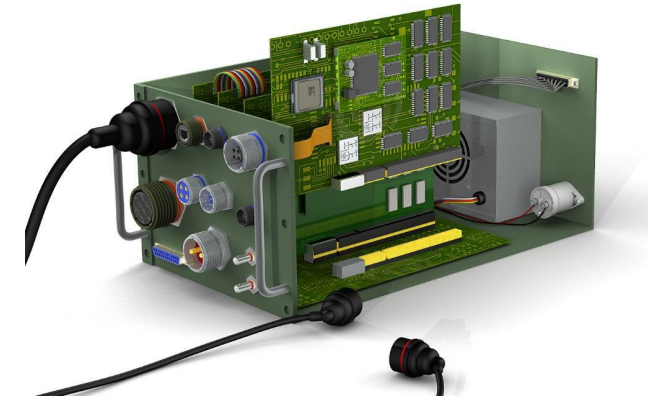
# Interconnect Standards – everyone's favorite subjects

## Topics:

- Key industry drivers and influence on connector development
- Status and trends in interconnect standards development
- How can we accelerate connector standardization and implementation
- What are the next challenges and opportunities

# Industry Drivers – Embedded Systems

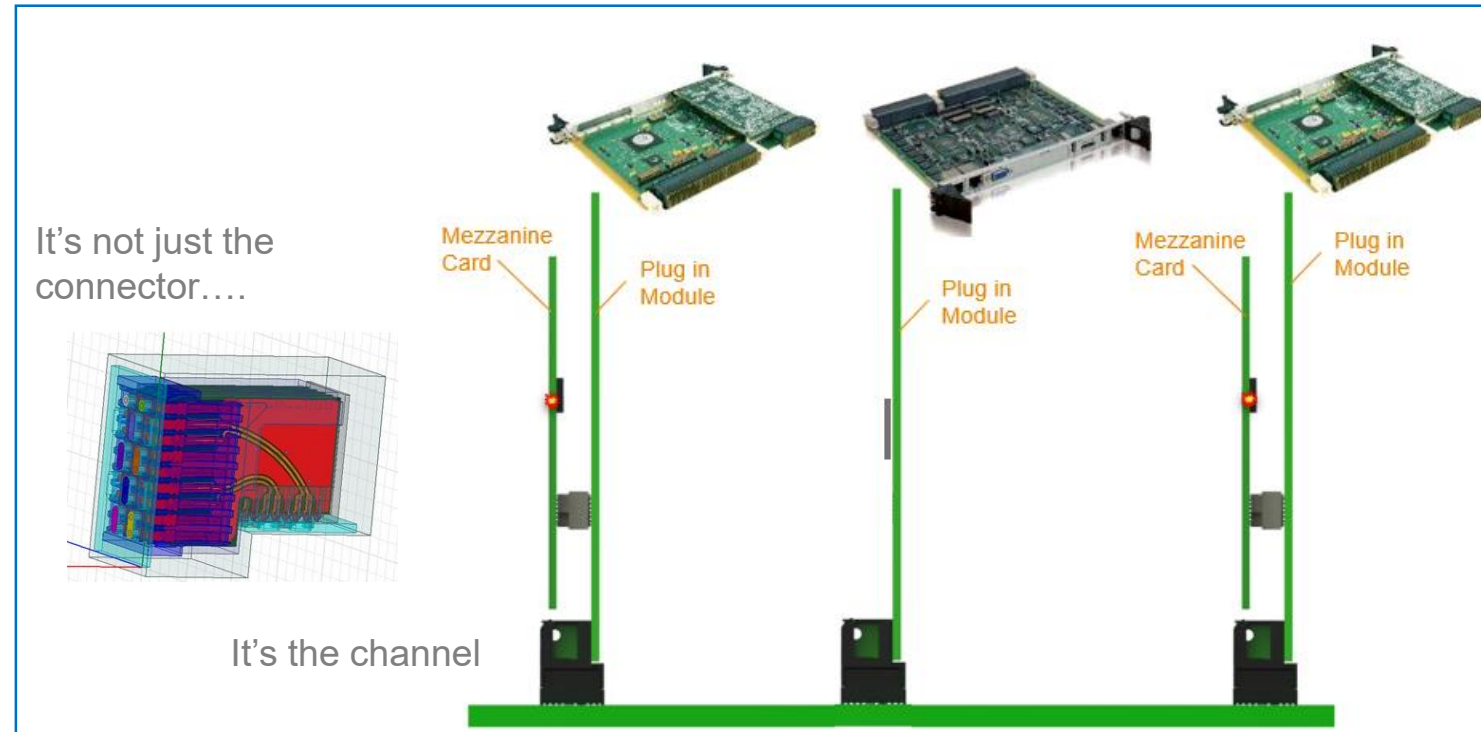
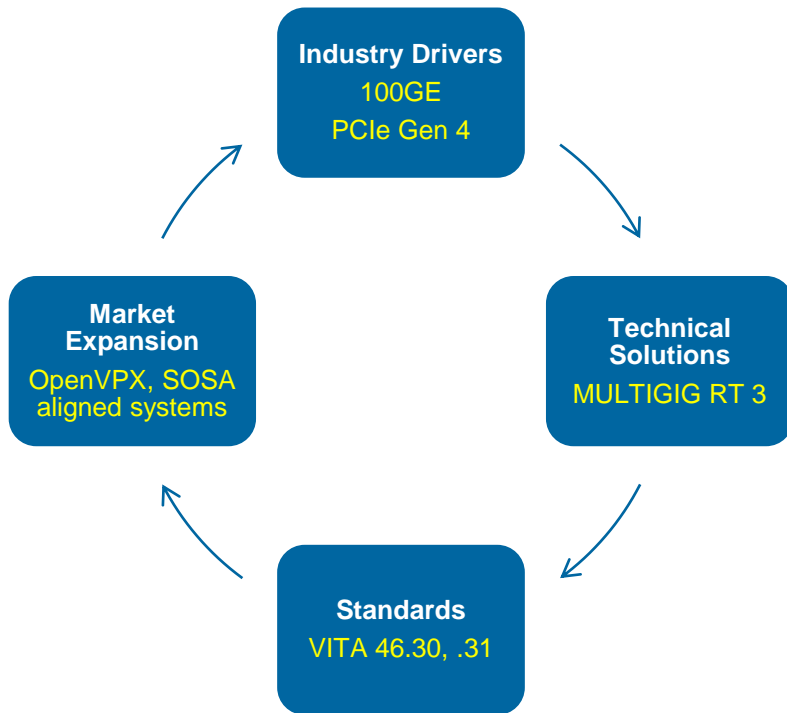
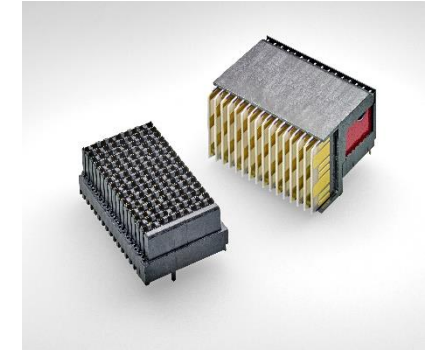
- Faster processors, more cores
- Increased I/O count and functionality within a plug-in module
- Reduced SWaP (Size Weight and Power)
  - smaller packaging
  - lighter weight solutions
  - more efficient power
- Open systems architecture
- Modular, scalable systems



# Speed

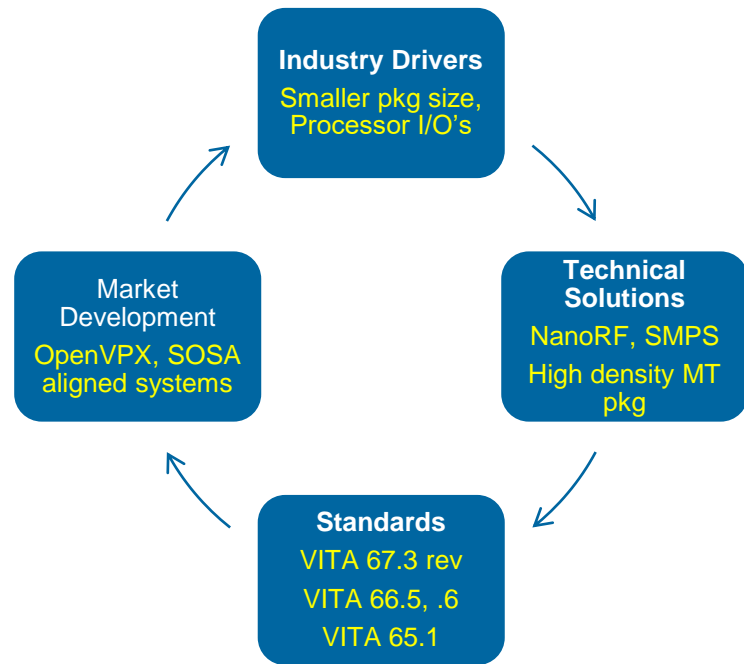
VITA 46 Backplane Connector:

From VPX release in 2006 aimed at 3.125 Gb/s...  
...to today's MULTIGIG RT 3 Connector at 25 Gb/s



# Density

Processors with more I/O, need for SWaP, are driving density requirements to unparalleled levels



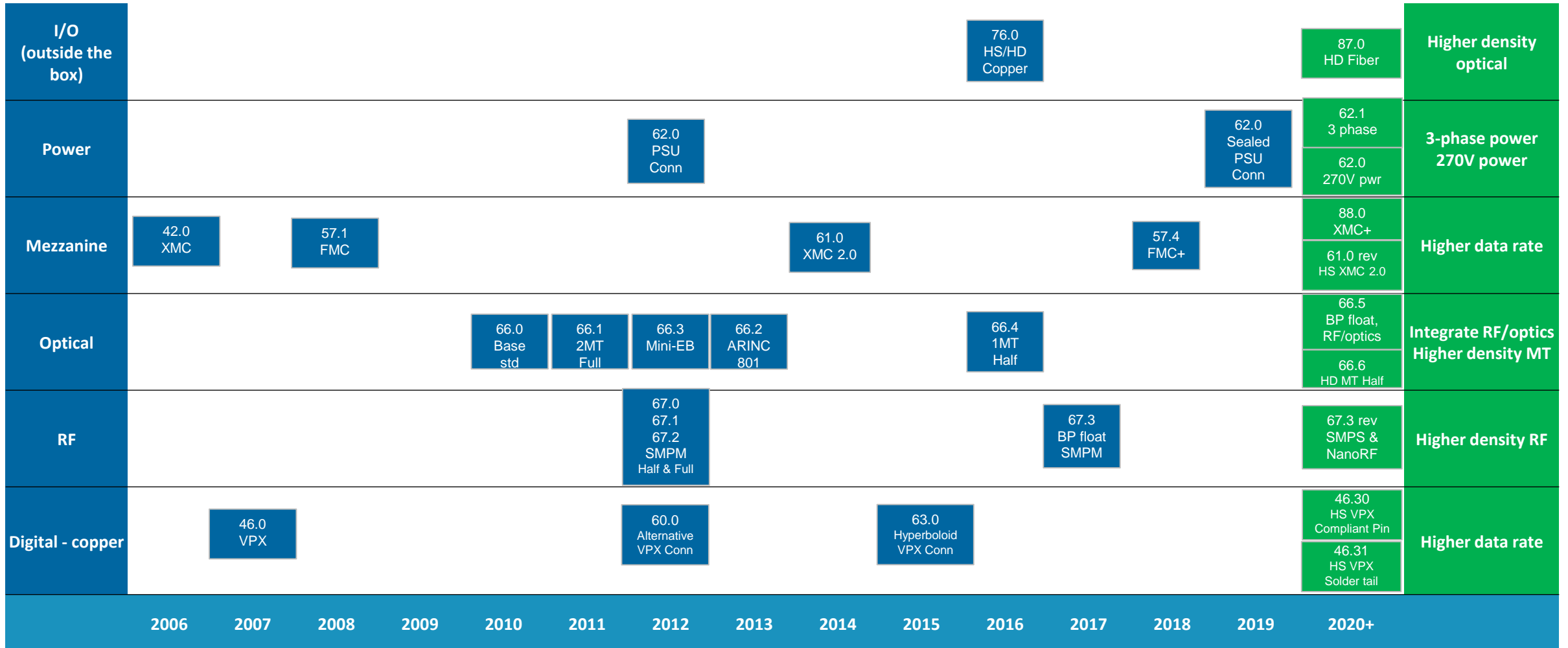
## The evolution of a 3U VPX slot interface

Today's Standards

Tomorrow's Standards... countless opportunities

<b>Digital</b>	32 diff pairs @ 10Gb/s	32 diff pairs @ 25Gb/s	48 diff pairs @ 25Gb/s
<b>Optical</b>	12-24 optical lanes @ 25Gb/s	24-48 optical lanes @ 25Gb/s	12-24 optical lanes @ 25Gb/s
<b>RF</b>	4 RF contacts @ 26.5 GHz	12 RF contacts @ 70 GHz	10 RF contacts @ 70 GHz

# The Evolution of VITA Interconnect Standards



Rapid technology changes are driving interconnect development for rugged embedded systems  
The window for next gen interconnect standards shrinks with each generation

# How Do We Accelerate Next Gen Standard Interconnects

*Build on existing interconnect standards – don't redefine the interface if we don't need to*

Standard MT interface  
(IEC 61754-5)



VITA 66 modules  
(cabled and transceiver)

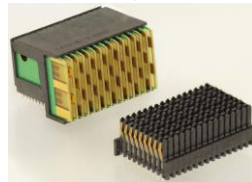


VITA 87 draft std with  
M38999 shells

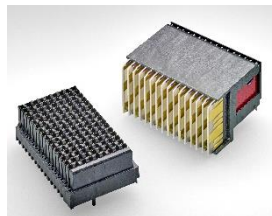
*Leverage commercial solutions for application in rugged embedded computing*



MULTIGIG RT 1 Connectors  
Used in data centers for "high speed" signals



MULTIGIG RT 2, 2-R Connectors  
10Gb/s  
VITA 46.0



MULTIGIG RT 3 Connectors  
25+ Gb/s  
VITA 46.30

*Establish "building blocks" that can be implemented for a range of system solutions*



NanoRF Modules  
VITA 67.3 rev



MT Modules  
VITA 66.x



Hybrid RF/Optical  
Module for highest  
density in a half module

VITA 66.5



# Flexibility vs Convergence in Standards



Building blocks support multiple configurations...



... but when is “multiple configurations” too many?



# Flexibility vs Convergence – RF/optical modules

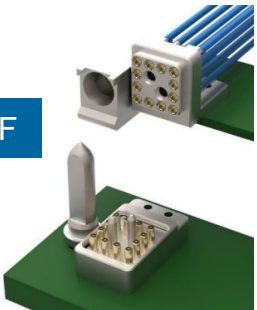
VITA 67.3 adds higher density interfaces NanoRF and SMPS and allows flexibility of contact positions (to be defined in VITA 65.1).

How do we maximize use of the module area for various use cases?

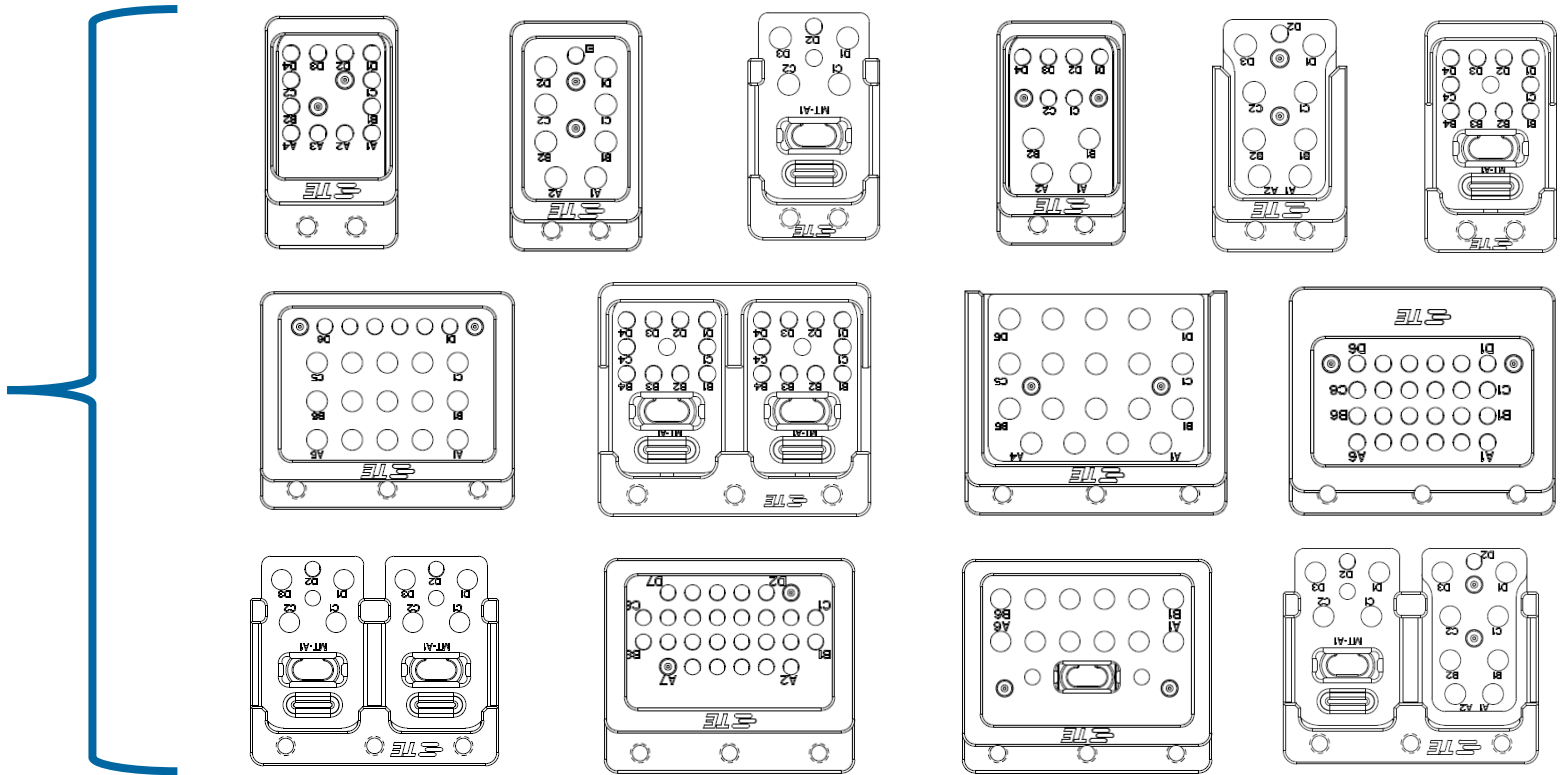
Numerous configurations and iterations were explored...



NanoRF



VITA 66



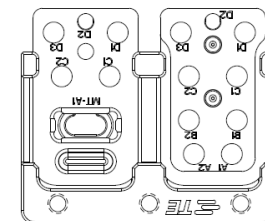
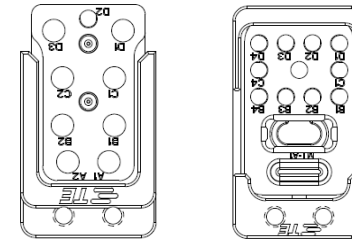
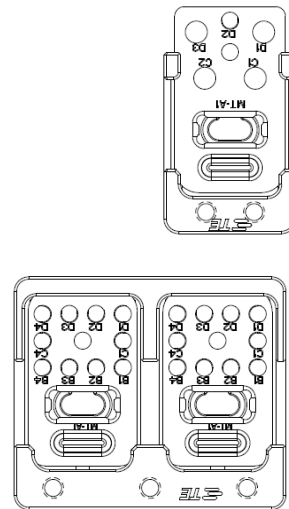
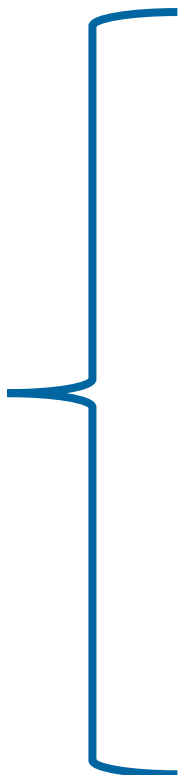
Building blocks allow for flexibility.



# Flexibility vs Convergence – RF/optical modules

SOSA™ (Sensors Open Systems Architecture) is aligning with several key designs to support 80% of use cases

Fewer, more common standard modules brings economies of scale, increases interoperability, shortens development cycles, reduces costs.



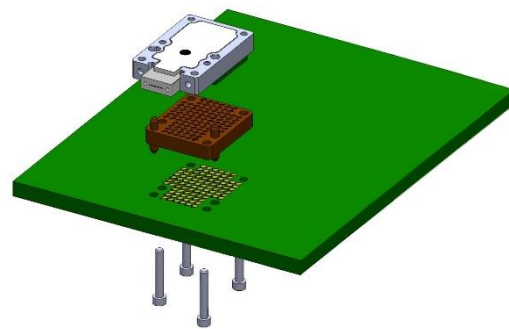
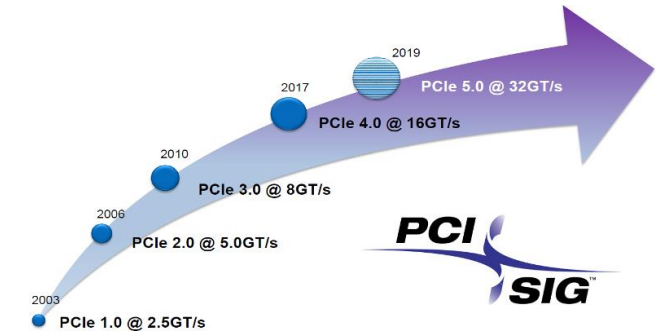
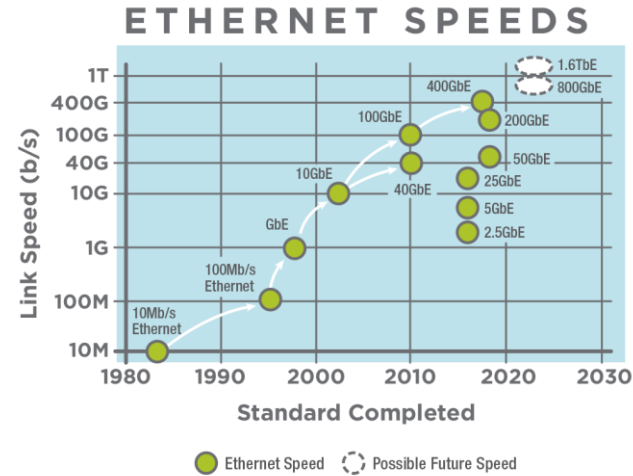
Standardizing the options brings economies of scale and interoperability.

# What will drive next gen interconnect standards?

## Speed

Ethernet, PCIe doubling data rates every 2-3 years

200G Ethernet, PCIe Gen 5 around the corner



Increased adoption of optics  
Higher fiber counts, higher speeds



Next Gen copper backplane interconnect?  
Cabled backplanes?



# What will drive next gen interconnect standards?

Speed

Density

How much more can we squeeze out of 3U VPX?  
Higher pin density backplane solutions?

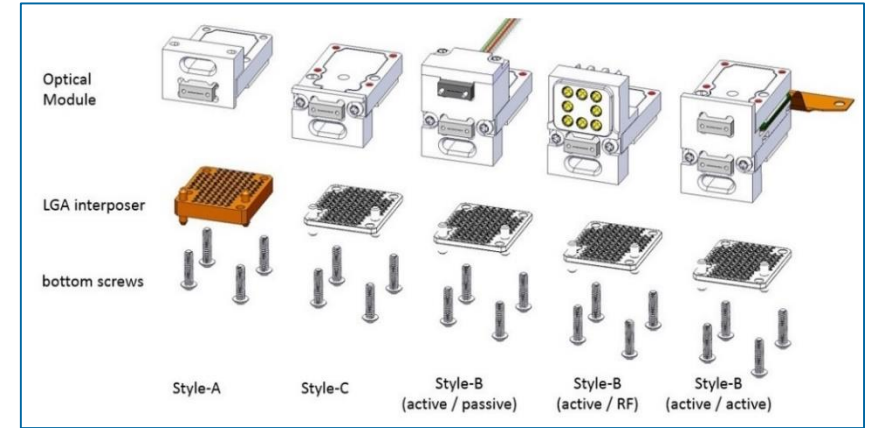
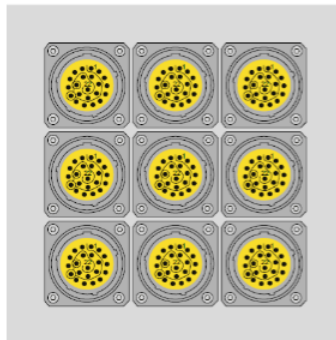
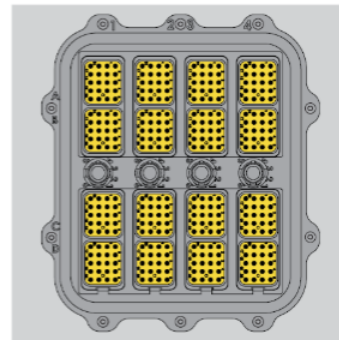


Image courtesy of Reflex Photonics

Rectangular I/O vs Circular?



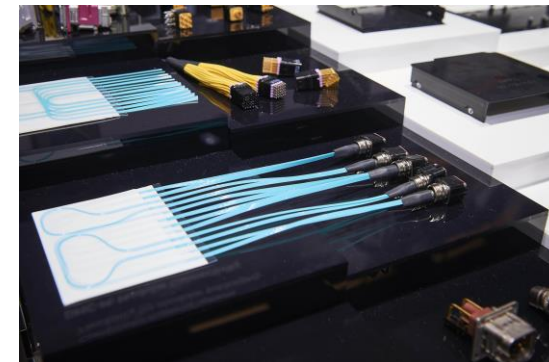
**Circular Connectors**  
Insert 13-35  
Size 22 Contacts, 5A  
198 contacts  
309 g (without panel)  
36 mounting screws  
9 panel cutouts



**DMC-M Connectors**  
Insert 20-22  
Size 22 Contacts, 5A  
320 contacts  
149 g (without panel)  
10 mounting screws  
1 panel cutout



Optical density... at the card edge and within a plug-in module



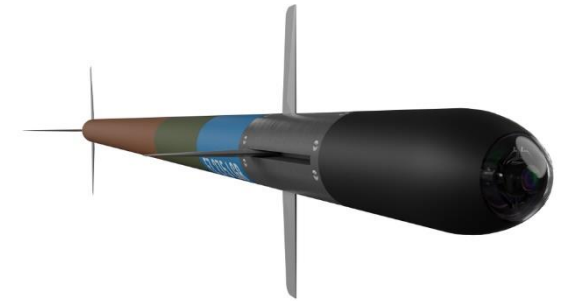
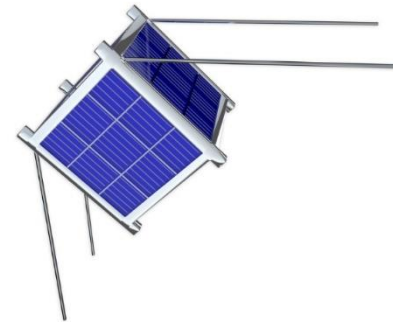
# What will drive next gen interconnect standards?

*Speed*

Small Form Factor (SFF) applications are growing...

*Density*

**Size**



... what will be the standard architecture for next gen SFF applications (smaller than 3U VPX)?

Image courtesy of Curtiss-Wright Corporation

# What will drive next gen interconnect standards?

*Speed*

*Density*

*Size*

**Power**

With increase in electrical systems over mechanical, voltages are increasing...

- 270VDC becoming more standard for aviation
- 600VDC ground vehicle systems
- 1000-1500VDC on the horizon

Power efficiency / density is more critical

... interconnect will need to support development in power supplies and power distribution systems



Standards development is challenging...

But needed...

- ... to support emerging technologies
- ... to build the ecosystem
- ... and to be a vital part of the industry development

And it has never been as active as it is today.



***Inventing. Connecting. Inspiring. Thriving.***

# Thank You

**SETTING THE STANDARD**

Increase power, data and bandwidth speed design with VITA open architecture solutions.



EVERY CONNECTION COUNTS

